

for several minutes in an inert or reducing ambient, in a process known as *sintering*. However, the use of pure aluminium can result in significant silicon diffusion into the aluminium layer during the sintering step. The resulting interface structure resembles the formation of aluminium spikes into the underlying silicon which may penetrate the doped junction (particularly if it is submicron in depth). This phenomenon is known as ‘junction spiking’.

The most reliable method for the elimination of junction spiking is the incorporation of a diffusion barrier layer between the aluminium and the silicon. This thin layer must be able to prevent significant diffusion at the sinter temperature, have low electrical resistivity and possess good adhesion properties to both the Si and Al (or whatever metal is being used as a contact). Two of the most common barrier layers are titanium tungsten (TiW) and titanium nitride (TiN), although a thin layer of TiSi_2 is required below TiN to reduce the contact resistance.

5.7 SUMMARY

The development of silicon photonic fabrication benefits greatly from the vast library of knowledge that already exists in the silicon microelectronics industry. In this chapter we have described the basic steps in the formation of an integrated silicon photonic device and acknowledge that we have merely glimpsed at the general area of silicon fabrication. Our emphasis has been skewed towards fabrication in academic and research environments where much of the near-term device development will be performed. We concede that as with any fast-moving technology, silicon photonic processing will find a path of least resistance which may make some of the processes described here redundant and necessitate the use of methods not described (for instance in the inevitable development of submicron devices). However, the overall process flow and much of the detail of this chapter will remain relevant for many years to come.

REFERENCES

1. M Quirk and J Serda (2001) *Semiconductor Manufacturing Technology*, Prentice-Hall, New Jersey.
2. S M Sze (1988) *VLSI Technology*, McGraw-Hill, Singapore.
3. G K Celler and S Cristoloveanu (2003) ‘Frontiers of silicon-on-insulator’, *J. Appl. Phys.*, **93**, 4955–4978.
4. J Schmidtchen, A Splett, B Schüppert and K Petermann (1991) ‘Low-loss single-mode optical waveguides with large cross-section in silicon-on-insulator’, *Electron. Lett.*, **27**, 1486–1487.

5. W P Maszara, G Goetz, A Caviglia and J B McKitterick (1988) 'Bonding of silicon wafers for silicon-on-insulator', *J. Appl. Phys.*, **93**, 4943–4950.
6. A F Evans, D G Hall and W P Maszara (1991) 'Propagation loss measurements in silicon-on-insulator waveguides formed by the bond-and-etchback process', *Appl. Phys. Lett.*, **59**, 1667–1669.
7. M Bruel (1995) 'Silicon on insulator material technology', *Electron. Lett.*, **31**, 1201–1202.
8. M Bruel, B Aspar and A-J Auberton-Hervé (1997) 'Smart-Cut: A new silicon on insulator material technology based on hydrogen implantation and wafer bonding', *Jpn J. Appl. Phys.*, **36**, 1636–1641.
9. T W Ang, G T Reed, A Vonsovici et al. (1999) '0.15 dB/cm loss in Uni-bond SOI waveguides', *Electron. Lett.*, **35**, 977–978.
10. *The International Technology Roadmap for Semiconductors*, Sematech (2001).
11. R A Soref, J Schmidtchen and K Pesermann (1991) 'Large single-mode rib waveguides in Ge-Si and Si-on-SiO₂', *IEEE J. Quant. Electron.*, **27**, 1971–1974.
12. U Fischer, T Zinke, J-R Kropp, F Andt and K Petermann (1996) '0.1 dB/cm waveguide losses in single-mode SOI rib waveguides', *IEEE Photon. Technol. Lett.*, **8**, 647–648.
13. B Jalali, P D Trinh, S Yegnanarayanan and F Coppinger (1996) 'Guided-wave optics in silicon-on-insulator technology', *IEE Proc. Optoelectron.*, **143**, 307–311.
14. A M Voshchenkov (1993) 'Plasma etching: an enabling technology for gigahertz silicon integrated circuits', *J. Vac. Sci. Technol. A*, **11**(4), 1211–1220.
15. C Y Chang and S M Sze (1996) *ULSI Technology*, McGraw-Hill, Singapore.
16. O Powell (2002) 'Single-mode conditions for silicon rib waveguides', *J. Lightwave Technol.*, **26**, 1851–1855.
17. A Rickman, G T Reed, B L Weiss and F Namavar (1992) 'Low-loss planar optical waveguides fabricated in SIMOX material', *IEEE Photonics Technol. Lett.*, **6**, 633–635.
18. B E Deal and A S Grove (1965) 'General relationship for the thermal oxidation of silicon', *J. Appl. Phys.*, **36**, 3770–3778.
19. C Jacobs, A Genis, L P Allen and P Roitman (1994) 'Effect of anneal temperature on Si/buried oxide interface roughness of SIMOX', *Proc. IEEE Int. SOI Conf.*, pp. 49–50.
20. K-S Chen, A Ayón and S M Spearing (2002) 'Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (DRIE)', *J. Micromech. Syst.*, **11**, 264–275.
21. L Lai and E A Irene (1999) 'Limiting Si/SiO₂ interface roughness resulting from thermal oxidation', *J. Appl. Phys.*, **86**, 1729–1735.

22. K L Lee, D R Lim, H-C Luan et al. (2000) 'Effect of size and roughness on light transmission in a Si/SiO₂ waveguide: experiment and model', *Appl. Phys. Lett.*, **77**, 1617–1619.
23. P D Hewitt and G T Reed (2000) 'Improving the response of optical phase modulators in SOI by computer simulation', *J. Lightwave Technol.*, **18**, 443–450.
24. J F Ziegler, J P Biersack and U Littmark (1985) *The Stopping and Range of Ions in Solids*, Pergamon, New York.
25. A P Knights, F Malik and P G Coleman (1999) 'The equivalence of vacancy-type damage in ion-implanted Si seen by positron annihilation spectroscopy', *Appl. Phys. Lett.*, **75**, 466–468.